WE CLAIM:

1. A non-volatile memory system, comprising:

a memory array including a plurality of memory cells in which each memory cell stores a data by threshold voltage corresponding to a first state and a second state, and a word line coupled to gates of the plurality of memory cells; and

a sequencer which controls procedures of changing the threshold voltage of the plurality of memory cells in response to corresponding commands;

wherein the plurality of memory cells includes a first group of memory cells having a threshold voltage corresponding to the first state, and a second group of memory cells having a threshold voltage corresponding to the second state;

wherein said sequencer includes an erase command procedure which puts the threshold voltage of the plurality of memory cells into the first state, and a write command procedure which puts the threshold voltage of at least a selected one of the first group of memory cells into the second state; and

wherein the write command procedure includes a first step in which the threshold voltage of the second group of memory cells is changed toward a voltage direction from the first state to the second state, and a second step in which the threshold voltage of the second group of memory cells and at least a selected one of the first group of memory cells are changed to the second state.

2. A non-volatile memory system according to claim 1, wherein in the first step, the threshold voltage of the first group of memory cells is changed toward the voltage direction from the first state to the second state while the threshold voltage of the second group of memory cells is changed toward the voltage direction from the first state to the second state.

3. A non-volatile memory system according to claim 2, wherein in the first step, the threshold voltage of the second group of memory cells is temporarily changed between the first state and the second state.

4. A non-volatile memory system according to claim 2, wherein in the first step, the threshold voltage of the second group of memory cells is temporarily changed to the first state.

5. A non-volatile memory system, comprising:

a memory array including

a plurality of memory cells in which each memory cell stores a data by threshold voltage corresponding to a first state and a second state;

a word line coupled to gates of the plurality of memory cells;

a plurality of data lines, each data line being coupled to each of the plurality of memory cells;

a plurality of sense latches, each sense latch being coupled to each of the plurality of data lines; and

a data input/output terminal coupled to the plurality of data lines; and

a sequencer which controls procedures of changing the threshold voltage of the plurality of memory cells in response to corresponding commands;

wherein the plurality of memory cells includes a first group of memory cells having a threshold voltage corresponding to the first state, and a second group of memory cells having a threshold voltage corresponding to the second state;

wherein said sequencer includes an erase command procedure which puts the threshold voltage of the plurality of memory cells into the first state, and a write command procedure which puts the threshold voltage of at least a selected one of the first group of memory cells into the second state; and

wherein the write command procedure includes a first step of storing a first data inputted from the input/output terminal to each of the plurality of sense latches; a second step of reading a second data from each of the plurality of memory cells onto each of the plurality of data lines, synthesizing a third data from the first data and the second data, and storing the third data in each of the plurality of sense latches; a third step of changing the threshold voltage of the plurality of memory cells toward a voltage direction from the second state to the first state; and a fourth step of putting into the second state the

threshold voltage of at least one of the memory cells indicated by the third data.

6. A non-volatile memory system according to claim 5, wherein the threshold voltage of the second group of memory cells is temporarily changed between the first state and the second state during the third step.

7. A non-volatile memory system according to claim 5, wherein the threshold voltage of the second group of memory cells is temporarily changed to the first state during the third step.

8. A non-volatile memory system, comprising:

a memory array including a plurality of memory cells in which each memory cell stores a data by threshold voltage corresponding to a first state and a second state, and a word line coupled to gates of the plurality of memory cells; and

a sequencer which controls procedures of changing the threshold voltage of the plurality of memory cells in response to corresponding commands;

wherein the plurality of memory cells includes a first group of memory cells having a threshold voltage corresponding to the first state, and a second group of memory cells having a threshold voltage corresponding to the second state;

wherein said sequencer includes an erase command procedure which puts the threshold voltage of the plurality of memory cells into the first state by applying a first voltage to the word line, and a first write command procedure which

puts the threshold voltage of at least one of the first group of memory cells into the second state by applying a second voltage to the word line; and

wherein said sequencer also includes a second write command procedure which puts the threshold voltage of at least one of the first group of memory cells into the second state by applying the first voltage and the second voltage to the word line.

9. A non-volatile memory system according to claim 8,

wherein the time required to apply the first voltage to the word line in the second write command procedure is shorter than the time required for the erase command procedure.

10. A non-volatile memory system according to claim 8,

wherein the threshold voltage of the second group of memory cells is temporarily changed between the first state and the second state by applying the first voltage to the word line during the second write command procedure.

11. A non-volatile memory system according to claim 8,

wherein the time required to apply the first voltage to the word line of the second write command procedure is substantially the same as the time required for the erasing command procedure.

12. A non-volatile memory system according to claim 8,

wherein the threshold voltage of the second group of memory cells is temporarily changed to the first state by

applying the first voltage to the word line during the second write command procedure.

13. A non-volatile memory system according to claim 8, wherein said memory array also includes

a plurality of data lines, each data line being coupled to each of the plurality of memory cells;

a plurality of sense latches, each sense latch being coupled to each of the plurality of data lines; and

a data input/output terminal coupled to the plurality of data lines;

wherein the second writing command procedure includes a first step of storing a first data inputted from the input/output terminal to each of the plurality of sense latches; a second step of reading a second data from each of the plurality of memory cells to each of the plurality of data lines, synthesizing a third data from the first data and the second data, and storing the third data into each of the plurality of sense latches; a third step of applying the first voltage to the word line and changing the threshold voltage of the plurality of memory cells toward a voltage direction from the second state to the first state; and a fourth step of applying the second voltage to the word line and putting into the second state the threshold voltage of at least one of the memory cells indicated by the third data.

14. A non-volatile memory system according to claim 13, wherein the time required for applying the first voltage to the word line of the second writing command procedure is shorter than the time required for the erase command procedure.

15. A non-volatile memory system according to claim 13, wherein the threshold voltage of the second group of memory cells is temporarily changed between the first state and the second state by applying the first voltage to the word line during the third step.

16. A non-volatile memory system according to claim 13, wherein the time required for applying the first voltage to the word line of the second writing command procedure is substantially the same as the time required for the erase command procedure.

17. A non-volatile memory system according to claim 13, wherein the threshold voltage of the second group of memory cells is temporarily changed to the first state by applying the first voltage to the word line during the third step.

18. A non-volatile memory system according to claim 1, wherein said memory system is a semiconductor device formed on a semiconductor substrate.

19. A non-volatile memory system according to claim 5,

wherein said memory system is a semiconductor device formed on a semiconductor substrate.

20. A non-volatile memory system according to claim 8, wherein said memory system is a semiconductor device formed on a semiconductor substrate.

21. A non-volatile memory system according to claim 1,

wherein said memory system is a memory card; and

wherein the memory card has a memory chip including said memory array and a control chip including said sequencer.

22. A non-volatile memory system according to claim 5,

wherein said memory system is a memory card; and

wherein the memory card has a memory chip including said memory array and a control chip including said sequencer.

23. A non-volatile memory system according to claim 8,

wherein said memory system is a memory card; and

wherein the memory card has a memory chip including said memory array and a control chip including said sequencer.

24. A non-volatile memory system according to claim 1, wherein said sequencer has a memory for storing the command procedures and conditions.

25. A non-volatile memory system according to claim 5, wherein said sequencer has a memory for storing the command procedures and conditions.

26. A non-volatile memory system according to claim 8, wherein said sequencer has a memory for storing the command procedures and conditions.

27. A non-volatile memory formed on a single semiconductor chip, comprising:

a plurality of memory cells, each memory cell including a transistor, storing information by threshold voltage of the transistor; and

a sequencer having a terminal to which commands are supplied, and controlling a corresponding procedure to put said plurality of memory cells into an erased state or a written state in response to each of the commands;

wherein said sequencer includes a command procedure which is started by one of the commands to perform an operation of putting the threshold voltage of said plurality of memory cells into a predetermined state; and

another operation of putting a part of said plurality of memory cells, which are in the written state before the one of the commands is supplied, and at least a selected one of said memory cells, which is selected from said plurality of memory cells after the one of the commands is supplied, into the written state.

28. A non-volatile memory according to claim 27, further comprising:

a word line to which said plurality of memory cells are respectively coupled.

29. A non-volatile memory according to claim 28, further comprising:

a data register coupled to said plurality of memory cells;

wherein after the one of the commands is applied, said data register stores first data for said plurality of memory cells on the basis of a second data read from said plurality of memory cells and a third data indicating the at least a selected one of said memory cells.

30. A non-volatile memory according to claim 29,

wherein the erased state has a first state of threshold voltage, and the written state has a second state of threshold voltage; and

wherein the threshold voltage of the part of said plurality of memory cells is temporarily between the first state and the second state during the command procedure.

31. A non-volatile memory according to claim 29,

wherein the erased state is the first state of threshold voltage, and the written state is the second state of threshold voltage; and

wherein the threshold voltage of the part of said plurality of memory cells is temporarily the first state during the command procedure.